WHAT IS CLAIMED IS:

1. A semiconductor package comprising:

a substrate comprising a plurality of bonding sites;

a semiconductor die on the substrate comprising a plurality of bond pads in electrical communication with the bonding sites;

a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing outer layer on the second metal layer; and

an encapsulant on the substrate encapsulating the die.

2. The semiconductor package of claim 1 further comprising a plurality of die contacts on the substrate in electrical communication with the external contacts, the die contacts comprising multi layer metal bumps bonded to the bond pads on the die.

3. The semiconductor package of claim 1 further comprising a plurality of die contacts on the substrate in electrical communication with the external contacts, and wherein the die is back bonded to the substrate and wire bonded to the die contacts.

4. The semiconductor package of claim 1 wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold.

5. The semiconductor package of claim 1 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

6. The semiconductor package of claim 1 wherein the die is wire bonded to the substrate in a chip-on-board configuration.

7. The semiconductor package of claim 1 wherein the die is wire bonded to the substrate in a board-on-chip configuration.

8. The semiconductor package of claim 1 wherein the substrate includes a recess and the die is contained in the recess in contact with a heat spreader.

9. A semiconductor package comprising:

a substrate comprising a board material;

a plurality of die contacts on the substrate and a plurality of external contacts on the substrate in electrical communication with the die contacts, each die contact and each external contact comprising a base metal layer, a bump metal layer and a non-oxidizing outer metal layer; and

a semiconductor die flip chip mounted to the substrate, the die comprising a plurality of bond pads bonded to the die contacts.

10. The semiconductor package of claim 9 further comprising an encapsulant on the substrate encapsulating the die.

11. The semiconductor package of claim 9 wherein the base metal layer comprises copper, the bump metal layer comprises nickel, and the non-oxidizing outer metal layer comprises gold.

12. The semiconductor package of claim 9 wherein each die contact and each external contact is generally pyramidal in shape with a planar tip portion.

13. The semiconductor package of claim 9 further comprising a solder mask on the substrate configured to electrically insulate the external contacts.

14. A semiconductor package comprising:

a substrate having a first side and an opposing second side;

a plurality of die contacts on the first side comprising first multi layered metal bumps having generally planar first tip portions;

a plurality of external contacts on the second side in electrical communication with the die contacts comprising second multi layered metal bumps having generally planar second tip portions; and

a semiconductor die flip chip mounted to the substrate, the die comprising a plurality of bond pads bonded to the die contacts.

15. The semiconductor package of claim 14 wherein each first multi layered metal bump and each second multi layered metal bump comprises a copper layer, a nickel layer and a gold layer.

16. The semiconductor package of claim 14 further comprising an encapsulant on the substrate encapsulating the die.

17. The semiconductor package of claim 14 wherein the die contacts have a pattern matching that of the bond pads on the die and the external contacts are in a grid array.

18. A semiconductor package comprising:

a substrate having a first side and an opposing second side;

a plurality of die contacts on the first side;

a plurality of bonding sites on the second side in electrical communication with the die contacts;

a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; and

a semiconductor die back bonded to the first side in a chip-on-board configuration, the die comprising a plurality of bond pads wire bonded to the die contacts.

19. The semiconductor package of claim 18 wherein the first metal layer comprises copper, the second metal layer comprises nickel and the non-oxidizing third metal layer comprises gold.

20. The semiconductor package of claim 18 further comprising an encapsulant on the substrate encapsulating the die.

21. The semiconductor package of claim 18 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

22. A semiconductor package comprising:

a substrate having a first side, an opposing second side and an opening;

a plurality of bonding sites on the second side and a plurality of conductors on the second side in electrical communication with the bonding sites;

a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer; and

a semiconductor die bonded to the first side in a board-on-chip configuration, the die comprising a plurality of bond pads aligned with the opening and wire bonded to the conductors.

23. The semiconductor package of claim 22 wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold.

24. The semiconductor package of claim 22 further comprising an encapsulant on the substrate encapsulating the die.

25. The semiconductor package of claim 22 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

26. A semiconductor package comprising:

a substrate having a first side, an opposing second side and a recess;

a plurality of bonding sites on the second side and a plurality of conductors on the second side in electrical communication with the bonding sites;

a plurality of external contacts on the bonding sites, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer;

a heat spreader in the recess; and

a semiconductor die in the recess in contact with the heat spreader, the die comprising a plurality of bond pads wire bonded to the conductors.

27. The semiconductor package of claim 26 further comprising an encapsulant in the recess encapsulating the die.

28. The semiconductor package of claim 26 wherein the first metal layer comprises copper, the second metal layer comprises nickel and the third metal layer comprises gold.

29. The semiconductor package of claim 26 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

30. A method for fabricating a semiconductor package comprising:

providing a substrate comprising a board material;

forming a plurality of bonding sites on the substrate;

depositing first metal layers on the bonding sites;

depositing second metal layers on the first metal layers;

depositing non-oxidizing third metal layers on the second metal layers to form external contacts for the package; and

mounting a semiconductor die to the substrate in electrical communication with the external contacts.

31. The method of claim 30 wherein the depositing the first metal layers step comprises electrolessly or electrolytically depositing copper on the bonding sites.

32. The method of claim 31 wherein the depositing the second metal layers step comprises electrolessly or electrolytically depositing nickel on the first metal layers.

33. The method of claim 32 wherein the depositing the third metal layers step comprises electrolessly or electrolytically depositing gold on the second metal layers.

34. The method of claim 30 further comprising forming a plurality of die contacts on the substrate comprising multi layered metal bumps and the mounting step comprises bonding the die to the die contacts in a flip chip configuration.

35. A method for fabricating a semiconductor package comprising:

providing a semiconductor die comprising a plurality of bond pads;

providing a substrate having a first side and an opposing second side;

forming a plurality of die contacts on the first side and a plurality of external contacts on the second side in electrical communication with the die contacts, each die contact and each external contact comprising a base metal layer, a bump metal layer, a non-oxidizing outer metal layer and a generally planar tip portion; and

mounting the die to the first side in a flip chip configuration with the bond pads bonded to the die contacts.

36. The method of claim 35 further comprising encapsulating the die.

37. The method of claim 35 wherein the base metal layer comprises copper, the bump metal layer comprises nickel and the non-oxidizing outer metal layer comprises gold.

38. The method of claim 35 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

39. The method of claim 35 wherein the forming step comprises electrolessly or electrolytically depositing the base metal layer, the bump metal layer and the non-oxidizing outer metal layer.

40. A method for fabricating a semiconductor package comprising:

providing a substrate comprising a board material having a first side and an opposing second side;

forming a plurality of first bonding sites on the first side and a plurality of second bonding sites on the second side in electrical communication with the first bonding sites;

depositing first metal layers on the first bonding sites and on the second bonding sites;

depositing second metal layers on the first metal layers;

depositing non-oxidizing third metal layers on the second metal layers to form a plurality of die contacts on the first side and a plurality of external contacts for the package on the second side; and

flip chip mounting a semiconductor die to the substrate by bonding the die to the die contacts.

41. The method of claim 40 wherein the flip chip mounting step comprises thermocompression bonding bond pads on the die to the die contacts.

42. The method of claim 40 wherein each of the depositing steps comprises electroless or electrolytic deposition.

43. The method of claim 40 further comprising encapsulating the die in an encapsulant.

44. The method of claim 40 wherein the first metal layers comprise copper, the second metal layers comprise nickel, and the third metal layers comprise gold.

45. The method of claim 40 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

46. A method for fabricating a semiconductor package comprising:

providing a semiconductor die comprising a plurality of bond pads;

providing a substrate having a first side and an opposing second side;

forming a plurality of die contacts on the first side;

forming a plurality of bonding sites on the second side in electrical communication with the die contacts;

forming a plurality of external contacts on the second side, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer;

mounting the die to the first side in a chip-on-board configuration; and

wire bonding the bond pads to the die contacts.

47. The method of claim 46 further comprising encapsulating the die in an encapsulant.

48. The method of claim 46 wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the third metal layer comprise gold.

49. The method of claim 46 wherein the substrate comprises a material selected from the group consisting of

bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

50. A method for fabricating a semiconductor package comprising:

providing a semiconductor die comprising a plurality of bond pads;

providing a substrate having a first side, an opposing second side and an opening;

forming a plurality of bonding sites on the second side and a plurality of conductors on the second side in electrical communication with the bonding sites;

forming a plurality of external contacts on the second side, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer;

mounting the die to the first side in a board-on-chip configuration with the bond pads aligned with the opening; and

wire bonding the bond pads to the conductors.

51. The method of claim 50 further comprising forming an encapsulant in the opening.

52. The method of claim 50 wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the third metal layer comprise gold.

53. The method of claim 50 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

54. A method for fabricating a semiconductor package comprising:

providing a semiconductor die comprising a plurality of bond pads;

providing a substrate having a first side, an opposing second side and a recess in the second side;

forming a plurality of bonding sites on the second side and a plurality of conductors on the second side in electrical communication with the bonding sites;

forming a plurality of external contacts on the second side, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing third metal layer on the second metal layer;

mounting the die in the recess in contact with a heat spreader; and

wire bonding the bond pads to the conductors.

55. The method of claim 54 further comprising forming an encapsulant in the recess.

56. The method of claim 54 wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the third metal layer comprise gold.

57. The method of claim 54 wherein the substrate comprises a material selected from the group consisting of bismaleimide-trizine (BT), epoxy resins, and polyimide resins.

58. An electronic assembly comprising:

a supporting substrate comprising a plurality of electrodes;

at least one semiconductor package on the supporting substrate comprising:

a substrate comprising a plurality of bonding sites;

a semiconductor die on the substrate comprising a plurality of bond pads in electrical communication with the bonding sites; and

a plurality of external contacts on the bonding sites bonded to the electrodes on the substrate, each external contact comprising a first metal layer on a bonding site, a second metal layer on the first metal layer, and a non-oxidizing outer layer on the second metal layer.

59. The assembly of claim 58 wherein the substrate and the package are configured as a multi chip module.

60. The assembly of claim 58 wherein the first metal layer comprises copper, the second metal layer comprises nickel, and the non-oxidizing outer layer comprises gold.

61. The assembly of claim 58 wherein the package further comprises a plurality of die contacts on the substrate in electrical communication with the external contacts, the die contacts comprising multi layer metal bumps bonded to the bond pads on the die.

62. An electronic assembly comprising:

a supporting substrate comprising a plurality of electrodes; and

a semiconductor package comprising a substrate, a plurality of die contacts on the substrate comprising first multi layered metal bumps having generally planar first tip portions, a semiconductor die bonded to the die contacts in a flip chip configuration, and a plurality of external contacts on the substrate in electrical communication with the die contacts comprising second multi layer metal bumps having generally planar second tip portions bonded to the electrodes.

63. The assembly of claim 62 wherein each die contact comprise a copper layer, a nickel layer and a gold layer.

64. The assembly of claim 62 wherein each external contact comprise a copper layer, a nickel layer and a gold layer.